AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 7, line 8 with the following ameded paragraph:

-- As shown in Fig. 3B, the node dielectric layer 346 over the conductive layer 348 is removed, followed by blanket deposition of the interval layer 349 in the trench and on the substrate, which in the interval layer 349 is preferably composed of TEOS. Referring to Fig. 3C, the interval layer ~~349a~~ 349 on the substrate and a portion of the interval layer ~~349a~~ 349 in the trench are removed by etching, in which the recessed top of the remaining interval layer 349a is preferably 1200nm~1800nm below the surface of the trench. As shown in Fig. 3D, a sacrificial layer 354 is conformally deposited, preferably is deposited by CVD to form an amorphous silicon with approximate thickness 20nm~70nm. As shown in Fig. 3E, the sacrificial layer 354 is etched by anisotropic etching, for example, a reactive ion etching or a dry etching with Cl as the main etchant. Thereafter, the sacrificial layer 354, over the interval layer 349a and the substrate, is etched, such that only the sacrificial layer 354 on sidewalls of the trench over the interval layer 349a remains.

Please replace the paragraph at page 9, line 28 with the following amended paragraph:

-- As shown in Fig. 4B, the node dielectric layer over the conductive layer is removed, followed by blanket deposition of the interval layer 449 in trench and on the substrate, in which the interval layer is preferably composed of TEOS. Referring to Fig. 4C, the interval layer ~~449a~~ 449 on the substrate and a portion of the interval layer ~~449a~~ 449 in the trench are removed by etching, in which the recessed top of the remaining interval layer 449a is preferably 1200nm~1800nm below the surface of the trench.